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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,430	12/28/2001	Alain Benayoun	FR920000071	1926

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EXAMINER	
LAM, DANIEL K	

ART UNIT	PAPER NUMBER
2667	12

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,430	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Daniel K Lam	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/28/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 3-8 are objected to as failing to comply with 37 CFR 1.84 because descriptive labels that are necessary for understanding the drawings are missing. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 5,361,255 issued to Diaz et al. in view of U. S. Pat. No. 6,195,335 issued to Calvignac et al.

Regarding claim 1, Diaz et al. discloses the claim limitations of an ATM transmission system comprising:

- A segment comprises an ATM cell payload 46, ATM header 48, and a switch header 50 (packet includes a header containing at least an address of a second LAN adapter to which the packet is forwarded). See fig. 2a, and col. 5, lines 26-28.
- An input interface 12, an output interface 14, a switching circuitry 16 which contains a space division matrix 32. The space division matrix contains a 3-stage crossbar basic switching elements BSEs 82. Each BSE supports 16 input ports and 16 output ports (NxN identical packet switch modules, each associates with m input ports and m output ports having rank k from 0 to N-1 to each column of N modules). See figures 1 and 2b, col. 4, lines 45-48, and col. 6, lines 4-8 and lines 12-20.

However Diaz et al. does not disclose the claim limitations that each pair of input port and output port defining a cross point at which is located a memory block for a data packet.

Calvignac et al. discloses a data patch switch comprises a switch fabric 100 having a crosspoint buffer 220 storing a data packet at the crosspoint. See fig. 2, and col. 3, lines 43-45.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to have a small memory block located at a crosspoint to store the packet to be switched for a couple of key motivations By having a small amount of memory at the crosspoint, and in corporation with the input and output schedulers, the switch can handle very high bursty traffic and can have very high throughput as taught by Calvignac et al. See col. 2, lines 44-50.

Regarding claim 2, in addition to disclose the claim limitations regarding claim 1 in the previous paragraphs, Calvignac et al. further discloses:

- A data patch switch comprises a switch fabric 100 having a crosspoint buffer 220 storing a data packet at the crosspoint (the memory block comprises a data memory unit for storing at least a data packet). See fig. 2, and col. 3, lines 43-45.
- Calvignac et al discloses that under the control of the input scheduler 310 and the gating signal on control line 260, the data packet is transferred into the crosspoint buffer 220. Similarly, under the control of the output scheduler 130 and gating signal on control line 270, the data packet is transferred to the output line 240. (A memory controller for storing the data packet, if the header contains the address of the output port, and reading the data for forwarding the data packet to the output port. See fig. 2, col. 4, lines 18-21, and lines 36-40.

Although neither Diaz et al. nor Calvignac et al. explicitly discloses a header validation control block for determining the address of the output port associated with the cross point, it is common practice to protect the address of the port in the packet header with CRC and validate the address is destination to the correct output port.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to have a header validation control to verify the address of the output port before using it. The key motivation being that, if there is an error in the address, the packet may go to a wrong output port and cause undesirable side effects.

Regarding claim 13, in addition to disclose the claim limitations regarding claim 1 discussed in the previous paragraphs, Diaz et al. further discloses that routing header comprising priority field 56 (header of the data packet an identification field for unicast and multicast), and routing tags 54, 58, and 60 (the second byte contains a module address field when said packet switch comprises several packet switch modules). See fig. 2a, col. 5, lines 32-35, and col. 7, table 1.

4. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 5,361,255 issued to Diaz et al. in view of U. S. Pat. No. 6,195,335 issued to Calvignac et al. in further view of U. S. Pat. No. 6,449,274 issued to Holden et al.

Regarding claims 4, 6, and 7, although Diaz et al. and to Calvignac et al. disclose the claim limitations regarding claim 1 discussed in the previous paragraphs, they do explicitly disclose the claim limitations of:

- An input control block connected to each input port for buffering a data packet before transmitting over a distributed data bus connected to all memory blocks (claim 4).
- Including an input memory unit (claim 4).
- A first memory controller for storing and reading said data packet before forwarding it over said distributed data bus (claim 4).
- Each down module includes an input expansion data block for buffering a data packet received from an expansion bus in connected to an up switch module (claim 6).

- Input expansion data block includes an expansion memory unit and a second memory controller for storing and reading said expansion memory unit before forwarding to said output port of said down switch module (claim 7).

Holden et al. disclose:

- An Input Routing Table IRT 120 receiving ATM cells from input transmission line 110 before forwarding them to the Switching Element SEs 150. See fig. 1, and col. 4, lines 38-42.
- The IRT 120 stores ATM cells in the IRT cell buffer 122. See fig. 2, and col. 4, lines 44-45.
- The IRT router controller 121 controls the function of the IRT 120. See fig. 2.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to have a self-routing crossbar packet switch with a small amount of data memory at the crosspoint; and have input buffer control and input cell storage separated from the switching function for couple of motivations. Firstly, by having a small amount of memory at the crosspoint, and in corporation with the input and output schedulers, the switch can handle very high bursty traffic and can have very high throughput as taught by Calvignac et al. See col. 2, lines 44-50. Secondly, by separating the input buffer control functions from the switching functions, specialized IC devices can be made for each function as taught by Holden et al. See col. 2, lines 43-46.

Regarding claim 3, in addition to disclose the claim limitations regarding claim 2 discussed in the previous paragraphs, Holden et al. further discloses that the output

routing table controller ORT 170 receives cells from the switch elements SEs 150, queues them in ORT cell buffer 172, and subsequently transmits onto a connecting output transmission line 180 (a scheduler is associated with each output port and causing the memory block to forward the data packet stored in the data memory unit to the output port). See figures 1 and 2, and col. 4, lines 49-51.

Regarding claim 5, in addition to disclose the claim limitations regarding claim 4 discussed in the previous paragraphs, Diaz et al. further discloses that a select 78 outputs the data packet to one of the two planes 70 or 72 (said input control block further includes a multiplexer for selecting either the output of said input memory unit or directly the bus connected to said input port when said input control block is not a first switch module). See fig. 2, and col. 5, lines 65-67.

Regarding claim 8, in addition to disclose the claim limitations regarding claim 3 discussed in the previous paragraphs, Holden et al. further discloses that a backpressure BP_ACK signal is transmitted back through arbiter 230 to the input port through BP_ACK drivers 295. Then the backpressure goes to the input routing table controller IRT 121 (a back-pressure mechanism which sends back-pressure signals to input adapters f to reduce the flow of the data packets transmitted to said packet switch when there is too much overflow detected by one or several schedulers of one of said switch modules). See fig. 3, and col. 7, lines 14-16.

Regarding claim 9, in addition to disclose the claim limitations regarding claim 8 discussed in the previous paragraphs, Holden et al. further discloses that in the output routing table controller, ORT, the priority back-pressure bit is derived from the near-fullness of queues 8-15 (an overflow mechanism receives overflow control signals from the schedulers when there is overflow and transmits an overflow signal to said back-pressure mechanism). See col. 29, lines 34-38.

Allowable Subject Matter

5. Claims 10-12 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel K. Lam whose telephone number is (703) 305-8605. The examiner can normally be reached on Monday-Friday from 8:30 AM to 4:30 PM.

   If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for this Group is (703) 872-9314.

   Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status Information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKL
March 20, 2004

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